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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/925,512	08/10/2001	Hideto Ohnuma	12732-068001	4989

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EXAMINER	
BOOTH, RICHARD A	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 03/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/925,512	OHNUMA ET AL.	
	Examiner	Art Unit	
	Richard A. Booth	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-85 is/are pending in the application.

4a) Of the above claim(s) See Continuation Sheet is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1,4,7,11,18,21,24,28,32-37,52-55,58,61,65-72 and 74-85 is/are rejected.

7)☒ Claim(s) 14 and 73 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 8/10/01 & 11/8/01.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims withdrawn from consideration are 2,3,5,6,8-10,12,13,15-17,19,20,22,23,25-27,29-31,38-51,56,57,59,60 and 62-64.

DETAILED ACTION

Election/Restrictions

Applicant's election of species I is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 7, 24, 34, 37, 61, 79-80, 82-83, and 85 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki, EP 1 003 223 A2 in view of Ishida, US 2001/0019127 A1.

Yamazaki shows the invention substantially as claimed including forming a conductive film 108 over a semiconductor 102 with an insulating film 103 therebetween; forming a resist pattern 109 on the conductive film; forming a gate electrode 108 by a first etching using the resist pattern wherein a thickness of an edge portion of the gate electrode is smaller than a thickness of a middle portion of the gate electrode; and introducing an impurity element into the semiconductor with the gate electrode as a mask to form a first impurity region and a second impurity region in the semiconductor 102, wherein the first impurity region is not overlapped with the gate electrode and the second impurity region is overlapped with the edge portion of the gate electrode (see figs. 1A-4D and paragraphs 0031-0073).

Yamazaki fails to expressly disclose wherein a thickness of an edge portion of the resist pattern is smaller than a thickness of a middle portion of the resist pattern.

Ishida discloses forming a gate electrode 15 having a taper shape using a resist pattern 17 wherein a thickness of an edge portion of the resist pattern is smaller than a thickness of a middle portion of the resist pattern (see figs. 4A-4C and paragraphs 0060-0070). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Yamazaki so as to form the tapered gate electrode structure using the method taught by Ishida because this is shown to be a suitable method in which to form tapered gate electrodes.

Claims 1, 7, 11, 18, 32, 35, 52, 54-55, 61, 65-71, and 79-85 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki, EP 1 003 223 A2 in view of Karr et al., U.S. Patent 6,534,425 B1.

Yamazaki shows the invention substantially as claimed including forming a conductive film 108 over a semiconductor 102 with an insulating film 103 therebetween; forming a resist pattern 109 on the conductive film; forming a gate electrode 108 by a first etching using the resist pattern wherein a thickness of an edge portion of the gate electrode is smaller than a thickness of a middle portion of the gate electrode; and introducing an impurity element into the semiconductor with the gate electrode as a mask to form a first impurity region and a second impurity region in the semiconductor 102, wherein the first impurity region is not overlapped with the gate electrode and the second impurity region is overlapped with the edge portion of the gate electrode (see figs. 1A-4D and paragraphs 0031-0073).

Yamazaki fails to expressly disclose wherein a thickness of an edge portion of the resist pattern is smaller than a thickness of a middle portion of the resist pattern and where the etching to form the tapered gate electrode is performed by dry etching.

Karr et al. discloses a reticle with a diffraction grating in order to form a tapered photoresist which can be transferred to an underlying structure through dry etching (see abstract, figs. 3a-5b and col. 3-line 23 to col. 4-line 42). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Yamazaki so as to use the reticle pattern and etching

process of Karr et al. because this is a suitable method in which to make a tapered gate electrode structure.

Claims 4, 21, 33, 36, 53, 58, 72 and 74-78 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki, EP 1 003 223 A2 in view of Karr et al., U.S. Patent 6,534,425 B1 as applied to claims 1, 7, 11, 18, 32, 35, 52, 54-55, 61, 65-71, and 79-85 above, and further in view of Tabata et al., U.S. Patent 5,744,381.

Yamazaki and Karr et al. are applied as above but fail to expressly disclose forming a reticle or a photoresist mask having a translucent film portion.

Tabata et al. discloses the use of a translucent mask such as silicon nitride for conventional chrome masks in photoresist applications (see col. 1-lines 58-64). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Yamazaki modified by Karr et al. so as to use the translucent mask of Tabata et al. because such a mask will improve the resolution characteristic of the exposure apparatus.

Allowable Subject Matter

Claims 14 and 73 are objected to as being dependent on a rejected claim, but would be allowable if written in independent form to include all the limitations of the present independent claim.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard A. Booth whose telephone number is (571) 272-1668. The examiner can normally be reached on Monday-Thursday from 7:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Richard A. Booth
Primary Examiner
Art Unit 2812